PVP 14

Code: IT4T5

II B.Tech - II Semester – Regular/Supplementary Examinations – April 2017

COMPUTER SYSTEM ARCHITECTURE
(INFORMATION TECHNOLOGY)

Duration: 3 hours Max. Marks: 70

PART – A

Answer ***all*** the questions. All questions carry equal marks

11 x 2 = 22

1.

a) Define bus. What is the role of bus?
b) Define micro operations.
c) What is the purpose of accumulator register?
d) List types of interrupts.
e) Define auto increment and auto decrement addressing modes.
f) Define control memory.
g) Define associate memory.
h) Define divide overflow. When it occurs?
i) What do you mean by strobe control?
j) What do you mean by parallel processing? How it is achieved using pipelining concept?
k) Define asynchronous serial transfer.

PART – B

Answer any ***THREE*** questions. All questions carry equal marks.

3 x 16 = 48 M

2. a) Explain all arithmetic micro operations. 8 M

   b) Write about three state bus buffers. 8 M

3. a) Explain about basic computer instructions and formats with example. 8 M

   b) Explain instruction cycle in detail. 8 M

4. a) Explain general register organization. 8 M

   b) Briefly write about micro programmed control organization. 8 M

5. a) Explain Booth algorithm for multiplication. 10 M

   b) Explain about memory hierarchy. 6 M

6. a) Explain the process of CPU - IOP communication. 8 M

   b) What is pipelining? Why it is used? Explain with an example. 8 M